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ATTORNEY DOCKET NO. 10030466-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Timothy L. Hillstrom

Serial No.: 10/698,278 **Examiner:** C. S. W. Tsai

Filing Date: October 31, 2005 **Group Art Unit:** 2857

Title: USING VECTOR NETWORK ANALYZER FOR ALIGNING OF TIME DOMAIN DATA

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on September 7, 2005 .

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) **$500.00**.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

☐	one month	$ 120.00
☐	two months	$ 450.00
☐	three months	$1020.00
☐	four months	$1590.00

☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **50-1078** the sum of $500.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-1078** pursuant to 37 CFR 1.25.

A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,

Timothy L. Hillstrom

By _____

Michael A. Papalas
Attorney/Agent for Applicant(s)

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(X) I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV482724485US, in an envelope addressed to: MS Appeal Brief-Patents, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450
Date of Deposit: **November 7, 2005**

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Docket No.: 10030466-1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Timothy L. Hillstrom

Application No.: 10/698,278 Confirmation No.: 1611

Filed: October 31, 2003 Art Unit: 2857

For: USING VECTOR NETWORK ANALYZER FOR ALIGNING OF TIME DOMAIN DATA Examiner: C. S. W. Tsai

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on September 7, 2005, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Agilent Technologies, Inc., a Delaware corporation having its principal place of business in Palo Alto, California.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 15 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 16-21
2. Claims withdrawn from consideration but not canceled: 0
3. Claims pending: 1-15
4. Claims allowed: 0
5. Claims rejected: 1-15

C. Claims On Appeal

The claims on appeal are claims 1-15.

IV. STATUS OF AMENDMENTS

Appellant did not file an Amendment After Final Rejection. The amendments made by the Response filed April 27, 2005 were entered and considered by the Examiner.

V. SUMMARY OF CLAIMED SUBJECT MATTER

According to claim 1, a method of using a vector network analyzer (VNA) for coordinated Voltage Standing-Wave Ratio (VSWR) and Time Domain Reflectometry (TDR) measurement, said method comprising:

configuring said VNA for identifying discontinuities correlated to a VSWR lobe.

According to claim 2, the method of claim 1 additionally comprising:

identifying a largest VSWR lobe in the frequency band of interest (Paragraph 0023; 304, Figure 3);

using phase data associated with S_{11} scattering parameter to find the correct electrical delay required to align Low Pass Step Transform data (Paragraph 0023; 304-307, Figure 3); and

configuring said Low Pass Step Transform span and center time to align coherent inductive and capacitive discontinuities relative to grid lines of a TDR display (Paragraph 0023; 308, Figure 3).

According to claim 3, the method of claim 2 additionally comprising:

setting a first channel to Low Pass Step Transform and a second channel to a scattering parameter S_{11} (Paragraph 0023; 303, Figure 3);

finding f_0, the frequency at the peak amplitude of the largest lobe of said scattering parameter S_{11} in the frequency band of interest (Paragraph 0023; 304, Figure 3);

setting electrical delay to zero (Paragraph 0023; 305, Figure 3);

finding the phase of S_{11} at f_0 (Paragraph 0023; 305, Figure 3);

denoting said phase θ (degrees) (Paragraph 0023; 306, Figure 3);

setting electrical delay in said first and said second channels to $(90-\theta)/(360*f_0)$, such that said S_{11} lobe phase reads 90 degrees(Paragraph 0023; 306, Figure 3);

setting said first channel span to $10/f_0$ (Paragraph 0023; 308, Figure 3);

setting said first channel center to 0.4*span (Paragraph 0023; 308, Figure 3); and

setting said first channel format to real (Paragraph 0023; 308, Figure 3).

According to claim 4, the method of claim 3 additionally comprising:

ensuring a valid 1-port calibration is performed on said VNA (Paragraph 0023; 302, Figure 3);

setting said first channel reference position to five divisions(Paragraph 0023; 308, Figure 3);

setting said first channel reference value to zero(Paragraph 0023; 308, Figure 3).; and

setting said first channel scale to 0.05 units per division (Paragraph 0023; 308, Figure 3).

According to claim 5, the method of claim 2 additionally comprising repeating said method for any additional problem VSWR lobes in said frequency band of interest, in order of decreasing lobe magnitude (Paragraph 0040, 615, Figure 6).

According to claim 6, the method of claim 2 further comprising calibrating the magnitudes of capacitive, inductive, and resistive discontinuities, thereby allowing the design of correctly sized compensating features (Paragraph 0029).

According to claim 7, the method of claim 3 wherein said method is performed manually (Paragraph 0042).

According to claim 8, the method of claim 3 wherein said method is performed automatically (Paragraph 0042).

According to claim 9, the method of claim 8 additionally comprising:

providing a suitable VNA (Paragraph 0042; 602, Figure 6);

placing by a user a user-scrollable display marker on a VSWR or S_{11} lobe of interest (Paragraph 0042; 603, Figure 6);

pressing a control key by said user, thereby initiating automated execution of said method (Paragraph 0042; 604, Figure 6); and

automatically displaying a Low Pass Step Transform with correct time alignment for identifying coherent, canceling, and orthogonal circuit discontinuities (Paragraph 0042; 606, Figure 6).

According to claim 10, the method of claim 9 wherein said suitable VNA comprises:

a visual display (Paragraph 0015; 11, Figure 1);

a processor operable to process time domain and frequency domain reflection signals for graphic presentation on said visual display, said processor capable of performing VNA state control and vector mathematical operations (Paragraph 0015; 16, Figure 1): and

wherein said display includes a visual display marker having a recognizable shape (Paragraph 0015).

According to claim 11, the method of claim 6, wherein said method is performed automatically (Paragraph 0042).

According to claim 12, the method of claim 11 additionally comprising:

providing a suitable VNA (Paragraph 0042; 602, Figure 6); and

calculating the relationship of discontinuity amplitude to excess capacitance and/or excess inductance using a processor associated with said VNA (Paragraph 0044).

According to claim 13, the method of claim 12 additionally comprising placing a user-scrollable display marker on a time-domain discontinuity (Paragraph 0042);

According to claim 14, the method of claim 12 additionally comprising accepting at a user interface of said VNA y-axis scaling unit inputs of pF per division and/or nH per division (Paragraphs 0033, 0039).

According to claim 15, the method of claim 12 additionally comprising selecting via a calibration enunciator of a TDR display of said VNA a scale in pF per division and/or nH per division in response to user interface entry of units per division (Paragraph 0044).

VI. GROUNDS OF OBJECTION TO BE REVIEWED ON APPEAL

A. First Ground of Rejection

Claims 1-15 are rejected under 35 U.S.C. § 101.

B. Second Ground of Rejection

Claim 1 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Tarczy-Hornoch et al.* (U.S. Patent No. 4,630,228, hereinafter *Tarczy*) in view of *Gumm* (U.S. Patent No. 6,437,578).

VII. ARGUMENT

A. First Ground of Rejection

Claims 1-15 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter. Regarding remaining claims 1-15, the Examiner states that these "recite no clearly defined practical application of the claimed method or do not draw a conclusion as to the final end result of configuring of a vector network analyzer (VNA) being directed toward a practical application." *See* Office Action, page 2, paragraph 3. 35 U.S.C. § 101 recites that "[w]hoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor...." Appellant can find no requirement of 35 U.S.C. § 101 that requires a claim recite a "clearly defined practical application."

A failure to disclose enough information about an invention to make its usefulness apparent can result in claims not meeting the requirements of 35 U.S.C. § 101. *See Brenner v. Manson*, 383 U.S. 519, 148 USPQ 689 (1966); *In re Ziegler*, 992 F.2d 1197, 26 USPQ2d 1600 (Fed. Cir. 1993). That is not the case here. Appellant respectfully asserts that claims 1-15 recite a useful process—"using a vector network analyzer (VNA) for coordinated Voltage Standing-Wave Ratio (VSWR) and Time Domain Reflectometry (TDR) measurement...." Claim 1 also comprises a limitation that suggests a use for such a process—"configuring said VNA for identifying discontinuities correlated to a VSWR lobe." Accordingly, claim 1 is

directed to subject matter that comprises a useful process, which is patentable under 35 U.S.C. § 101.

The Examiner also "submits that the claimed method merely manipulates an abstract idea without limitation to a practical application." *See* Office Action, page 2, paragraph 3. Appellant respectfully traverses the Examiner's submission that the claimed method "merely manipulates an abstract idea without limitation to a practical application." While abstract ideas may not be patentable, the subject matter of claims 1-15 is a process that comprises using a vector network analyzer, which Appellant respectfully asserts is not abstract.

For the reasons shown above, Appellant respectfully asserts that the Examiner has not provided a proper rejection of claims 1-15 under 35 U.S.C. § 101. Appellant requests that the rejection of these claims be withdrawn and claims 1-15 passed to allowance.

B. Second Ground of Rejection

Claim 1 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Tarczy* in view of *Gumm*.

To establish a prima facie case of obviousness, *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991), teaches that three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Without conceding that the proposed combination meet any of the remaining criteria for establishing an obviousness rejection, the Appellant respectfully asserts that the combination of *Tarczy* and *Gumm* does not teach or suggest all of the limitations of claim 1.

Claim 1 recites "[a] method of using a vector network analyzer (VNA) for coordinated Voltage Standing-Wave Ratio (VSWR) and Time Domain Reflectometry (TDR) measurement, said method comprising configuring said VNA for identifying discontinuities

correlated to a VSWR lobe." *Tarczy* teaches a transmission line analyzer "comprising frequency domain reflectometer means." *See* col. 1, line 65. The claims of *Tarczy* are also directed to frequency domain reflectometer means. *See* col. 12, lines 42, 62; col. 13, line 13; col. 14, line 7. *Tarczy* does not appear to teach or suggest identifying discontinuities correlated to a VSWR lobe. Accordingly, *Tarczy* does not teach or suggest at least the claim 1 limitation of "identifying discontinuities correlated to a VSWR lobe."

Gumm is not relied upon as curing the deficiencies of *Tarczy* with respect to claim 1. Accordingly, *Tarczy* in view of *Gumm* does not teach or suggest at least the claim 1 limitation of "identifying discontinuities correlated to a VSWR lobe."

Because the cited combination of references does not teach or suggest all limitations of claim 1, claim 1 is not obvious over the cited references. Appellant respectfully requests that the rejection of record be withdrawn and claim 1 passed to allowance.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A do include the amendments filed by Appellant on April 27, 2005.

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV482724485US, in an envelope addressed to: MS Appeal Brief-Patents, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Date of Deposit: November 7, 2005

Typed Name: Susan Bloomfield

Signature: Susan Bloomfield

Respectfully submitted,

By _____

Michael A. Papalas
Attorney/Agent for Applicant(s)
Reg. No.: 40,381

Date: November 7, 2005

Telephone No. (214) 855-8186

APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/698,278

1. (Previously Presented) A method of using a vector network analyzer (VNA) for coordinated Voltage Standing-Wave Ratio (VSWR) and Time Domain Reflectometry (TDR) measurement, said method comprising:

configuring said VNA for identifying discontinuities correlated to a VSWR lobe.

2. (Original) The method of claim 1 additionally comprising:

identifying a largest VSWR lobe in the frequency band of interest;

using phase data associated with S_{11} scattering parameter to find the correct electrical delay required to align Low Pass Step Transform data; and

configuring said Low Pass Step Transform span and center time to align coherent inductive and capacitive discontinuities relative to grid lines of a TDR display.

3. (Original) The method of claim 2 additionally comprising:

setting a first channel to Low Pass Step Transform and a second channel to a scattering parameter S_{11};

finding f_0, the frequency at the peak amplitude of the largest lobe of said scattering parameter S_{11} in the frequency band of interest;

setting electrical delay to zero;

finding the phase of S_{11} at f_0;

denoting said phase θ (degrees);

setting electrical delay in said first and said second channels to $(90-\theta)/(360*f_0)$, such that said S_{11} lobe phase reads 90 degrees;

setting said first channel span to $10/f_0$;

setting said first channel center to 0.4*span; and

setting said first channel format to real.

4. (Original) The method of claim 3 additionally comprising:

ensuring a valid 1-port calibration is performed on said VNA;

setting said first channel reference position to five divisions;

setting said first channel reference value to zero; and

setting said first channel scale to 0.05 units per division.

5. (Original) The method of claim 2 additionally comprising repeating said method for any additional problem VSWR lobes in said frequency band of interest, in order of decreasing lobe magnitude.

6. (Original) The method of claim 2 further comprising calibrating the magnitudes of capacitive, inductive, and resistive discontinuities, thereby allowing the design of correctly sized compensating features.

7. (Original) The method of claim 3 wherein said method is performed manually.

8. (Original) The method of claim 3 wherein said method is performed automatically.

9. (Original) The method of claim 8 additionally comprising:

providing a suitable VNA;

placing by a user a user-scrollable display marker on a VSWR or S_{11} lobe of interest;

pressing a control key by said user, thereby initiating automated execution of said method; and

automatically displaying a Low Pass Step Transform with correct time alignment for identifying coherent, canceling, and orthogonal circuit discontinuities.

10. (Original) The method of claim 9 wherein said suitable VNA comprises:

a visual display;

a processor operable to process time domain and frequency domain reflection signals for graphic presentation on said visual display, said processor capable of performing VNA state control and vector mathematical operations: and

wherein said display includes a visual display marker having a recognizable shape.

11. (Original) The method of claim 6, wherein said method is performed automatically.

12. (Original) The method of claim 11 additionally comprising:

providing a suitable VNA; and

calculating the relationship of discontinuity amplitude to excess capacitance and/or excess inductance using a processor associated with said VNA.

13. (Original) The method of claim 12 additionally comprising placing a user-scrollable display marker on a time-domain discontinuity;

14. (Original) The method of claim 12 additionally comprising accepting at a user interface of said VNA y-axis scaling unit inputs of pF per division and/or nH per division.

15. (Original) The method of claim 12 additionally comprising selecting via a calibration enunciator of a TDR display of said VNA a scale in pF per division and/or nH per division in response to user interface entry of units per division.

16-21. (Canceled)